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PG III Semester

Unit - Serial in-Serial out Shift Register

## Serial in - Serial out shift Register

The flip-flops used to construct registers are either J-K or D-type. In fig 3. four J-K flip flops wired as a four bit register are shown. They are connected such that the out-put of FF/A transfer into FF/B, the output of FF/B into FF/C

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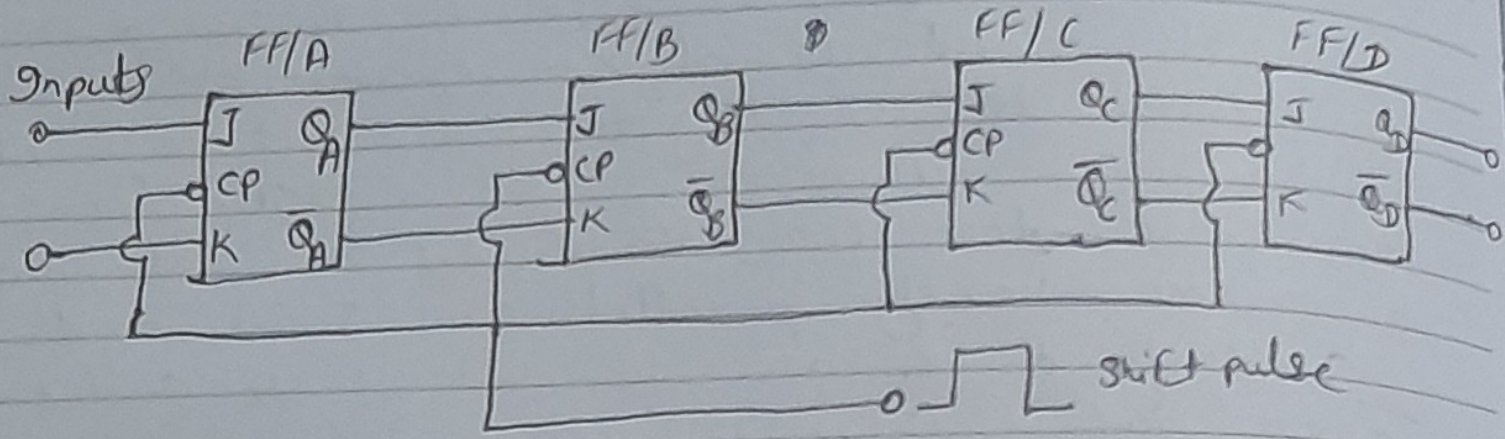
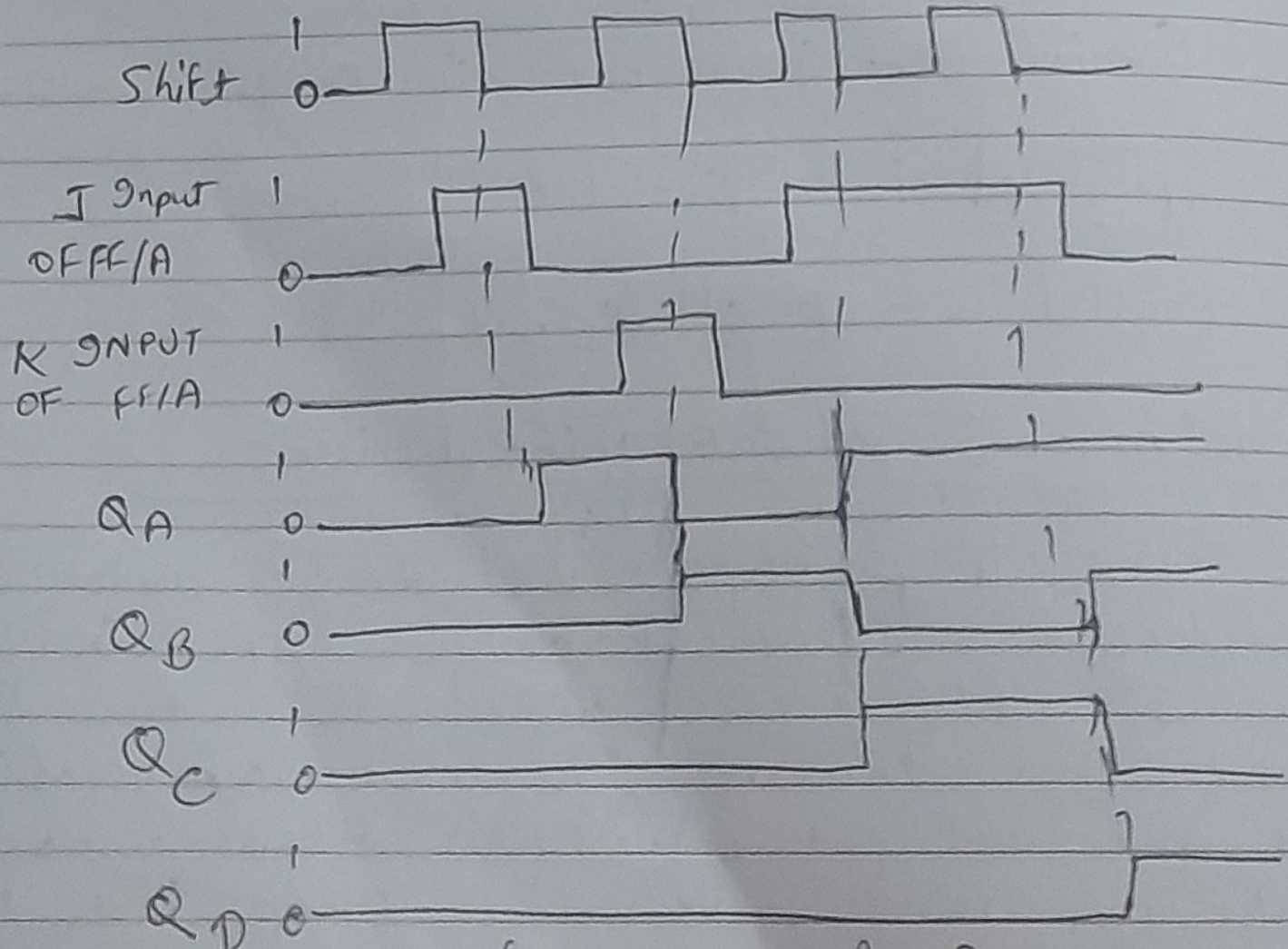
and of FF/C into FF/D. Thus on the application of a shift pulse, each flip flop takes on data bit that was stored previously in the flip flop on the left.




four bit Shift Register

fig: (3)

The data bit to be shifted into the flip-flop must be present at the JK, inputs. Since the data bit is either a 1 or a 0, there are two cases of J, K logic levels:

(i) To shift a 0 into the flip-flop, J=0, and K=1

(ii) To shift a 1 into the flip-flop, J=1 and K=0. These logic levels can change at positive going edge or negative going edge (called falling edge, or negative clock transition) of the clock pulse. Thus J, K inputs are controlled by the clock pulse and are termed as clock inputs. In four bit shift register, shown in fig (3), master-slave JK flip flops, having clock inputs that change at the falling edge of clock pulse, have been used. The clock pulse at which clock inputs change, is called a shift pulse.

When shift pulse occurs $Q_A$ takes on a value determined by the conditions present on its J and K inputs, let J=1 and K=0. We assume that all flip-flops are initially in 0 state before the first shift pulse is applied. From waveforms of fig (3) we note that:

(i) When first shift pulse is applied then all flip-flops have J=0 (low) and K=1 (high) except for FF/A which has J=1, K=0. Thus on the falling edge of the shift pulse, only $Q_A$ goes to 1, while all other flip-flops stay low. Now at the input of FF/B, there is J=1, K=0.

(ii) When second shift pulse occurs then it finds that FF/B has J=1, K=0 and all other flip-flops have J=0, K=1 so that at the falling edge of second shift pulse, only $Q_B$ goes high (a 1). Now at the input of FF/C, there is J=1, K=0.

(iii) When third shift pulse occurs, then it finds that FF/C has J=1, K=0 so that at the falling edge of third shift pulse, $Q_C$ goes to a 1. Now at the input of FF/D, there is J=1, K=0

(iv) When fourth shift pulse occurs, then it finds that FF/D has J=1, K=0 so that at the falling edge of fourth shift pulse, $Q_D$ goes to a 1.

Thus FF/A input J=1, K=0 is transferred to FF/D output on the application of four clock pulses.

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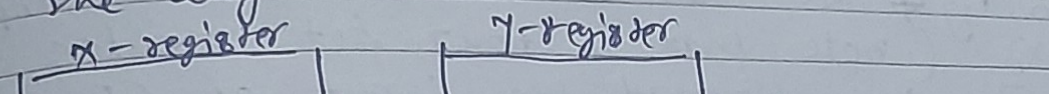
# Serial Transfer between Registers:

What described above was the shifting from one flip-flop to another in a shift register, say X. The data can be serially shifted to another register, say Y fig ③, in the way



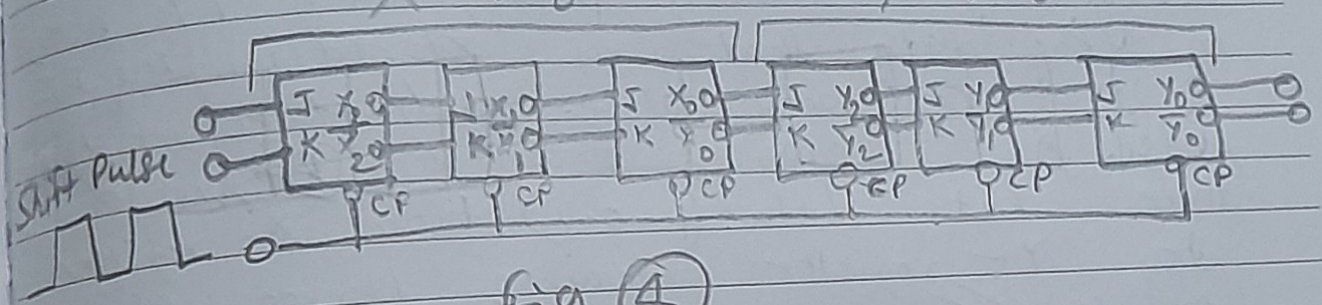




fig ④

| $X_2$ | $X_1$ | $X_0$ | $Y_2$ | $Y_1$ | $Y_0$ | |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | ← Before Shift Pulse |
| 1 | 1 | 0 | 1 | 0 | 0 | ← After first Pulse |
| 0 | 1 | 1 | 0 | 1 | 0 | ← After second Pulse |
| 0 | 0 | 1 | 1 | 0 | 1 | ← After third Pulse |
| 0 | 0 | 0 | | | | |

fig ⑤

Suppose, before any shift pulse is applied, contents of X- register are 1-0-1 (i.e $x_2 = 1$, $x_1 = 0$, $x_0 = 1$) and that of Y-register is 0-0-0. As the shift pulses are applied states of each FF will change as shown in fig 4. We use J=0 and K=1 as input at $x_2$ (note that in four bit register, we used J=1, K=0 at the input of FF/A) so that $x_2$ will go low (a 0) on the application of first pulse and will stay there. On falling edge of each pulse, each FF takes on the data that was stored in the FF to its left before the application of the pulse. As is obvious from fig (5), in a three bits data (1-0-1) from X- register to Y- register requires three shift pulses.